CLAIMS

1. An apparatus comprising:

a first circuit configured to present a first data signal and a first indicator signal in response to a first clock signal and an enable signal; and

a second circuit configured to present a second data signal and a second indicator signal in response to said first data signal, said first indicator signal and a second clock signal.

2. The apparatus according to claim 1, wherein said first indicator signal indicates when said first data signal is valid and said second indicator signal indicates when said second data signal is valid.

3. The apparatus according to claim 1, wherein said first clock signal comprises a first logic domain clock signal and said second clock signal comprises a second logic domain clock signal.

4. The apparatus according to claim 3, wherein (i) said apparatus is configured to synchronize said second data signal to

said second logic domain and (ii) said second data signal comprises said first data signal synchronized to said second domain.

5. The apparatus according to claim 1, wherein said first and second clock signals operate at the same frequency.

6. The apparatus according to claim 1, wherein said first and second clock signals operate out of phase with each other.

7. The apparatus according to claim 1, wherein (i) said first circuit is configured to store said first data signal until a new data signal is received and (ii) said second circuit is configured to store said second data signal until said second circuit receives said first data signal.

8. The apparatus according to claim 1, wherein said first circuit comprises:

a logic gate configured to (i) receive said first clock signal and said enable signal and (ii) present a gated clock signal;

a first register circuit configured to store and present said first data signal in response to said gated clock signal; and

a second register circuit configured to generate said first indicator signal in response to said gated clock signal and an inverse of said first indicator signal.

9. An apparatus according to claim 1, wherein said second circuit comprises:

a first register circuit configured to generate said second data signal in response to said second clock signal and said first data signal;

a second register circuit configured to generate a first intermediate indicator signal in response to said second clock signal and said first indicator signal;

a third register circuit configured to generate a second intermediate indicator signal in response to said second clock signal and said first intermediate indicator signal; and

a logic gate configured to generate said second indicator signal in response to said first and second intermediate indicator signals.

10. The apparatus according to claim 8, wherein (i) said logic gate comprises an AND gate and (ii) said first and second register circuits comprise D-type flip-flop circuits.

11. The apparatus according to claim 9, wherein (i) said first, second, and third register circuits comprise D-type flip-flop circuits and (ii) said logic gate comprises an EXCLUSIVE-OR gate.

12. The apparatus according to claim 1, wherein said apparatus is implemented integral to a member selected from a group consisting of an application specific integrated circuit, a CPLD and a FPGA.

13. The apparatus according to claim 1, wherein said first and second data signals comprise n-bit wide digital signals, where n is an integer.

14. An apparatus comprising:

means for presenting a first data signal and a first indicator signal in response to a first clock signal and an enable signal; and

means for presenting a second data signal and a second indicator signal in response to said first data signal, said first indicator signal and a second clock signal, wherein said second indicator signal is configured to indicate when said second data signal is synchronized from a first logic domain to a second logic domain.

15. A method of indicating data is synchronized from a first logic domain to a second logic domain comprising the steps of:

(A) presenting a first data signal and a first indicator signal in response to a first clock signal and an enable signal; and

(B) presenting a second data signal and a second indicator signal in response to said first data signal, said first indicator signal and a second clock signal.

16. The method according to claim 15, wherein said first clock signal comprises a clock signal of said first logic domain and said second clock signal comprises a clock signal of said second logic domain.

17. The method according to claim 15, wherein said method further comprises the step of operating said first and second clock signals at the same frequency.

18. The method according to claim 15, wherein said method further comprises the step of operating said first and second clock signals out of phase with each other.

19. The method according to claim 15, wherein said method comprises the step of implementing said method in a member of a group consisting of an application specific integrated circuit, a CPLD and a FPGA.

20. The method according to claim 15, wherein said first and second data signals comprise n-bit wide digital data signals, where n is an integer.